REMARKS

This communication is in response to the Final Office Action of August 15, 2006. In the Final Office Action, claims 20-27 were rejected.

Claims 20 through 27 are pending in the application.

Claims 20 and 24 are amended. The amendments to the claims do not add new matter.

Reconsideration is requested

Rejections under 35 U.S.C. § 102

Claims 20 through 27 were rejected under 35 U.S.C. § 102(e) over Tavana (U.S. Patent No. 5,825,202)

The § 102 rejection is improper for at least the following reasons.

Tavana discloses an integrated circuit with field programmable and application specific logic areas. The combined circuit includes a field programmable gate array (FPGA) portion and a mask-defined application-specific logic area (ASLA). According to Tavana:

> the ***mask-defined*** ASLA section reduces cost and renders the entire monolithic integrated circuit device more suitable for high volume production.

Tavana, col. 3, lines 13-14 (emphasis added). In addition, Tavana states that an advantage of the combined chip is that:

> a single novel structure, a ***mask-defined or otherwise permanent custom chip architecture*** with an FPGA device having a field-programmable architecture [is provided].

Tavana, col. 3, lines 35-37. Therefore, the circuit disclosed in Tavana includes the mask-defined ASLA portion that is mask-defined or otherwise permanent or custom. Accordingly, Tavana does not disclose "providing a semi-fabricated semiconductor wafer that lacks a metal one layer and on which has been formed a plurality of circuits that comprise a logic design and at least one programmable circuit capable of performing at least one of a plurality of logic transfer functions upon programming."

In addition, Tavana discloses a circuit that has a mask-defined ASLA portion with a ***mask-defined layer*** that is not modifiable because the ASLA portion is "mask-defined or otherwise [a] permanent custom chip architecture." Therefore, Tavana does not disclose "determining desired changes in the metal one layer needed to implement the modifications in the logic design, including connecting the at least one programmable circuit to the plurality of circuits" because modifications are not made to the mask-defined layer of the mask-defined ASLA portion.

Furthermore, because the mask-defined ASLA portion is permanent in Tavana, Tavana does not disclose "forming a metal one layer on said semi-fabricated semiconductor wafer in the same location as the metal one layer of the original specimen but having a configuration different from the metal one layer of the original specimen to effect the desired changes."

Moreover, the FPGA portion of the circuit disclosed in Tavana is programmable after the device is fabricated and can be programmed by routing using "a first matrix of programmable interconnects 28 and a second matrix of mask-defined interconnections 30." Tavana, col. 6, lines 7-10. When the FPGA portion is configured after the initial fabrication, however, Tavana does not disclose that a circuit with the FPGA complete with interconnects 28/30 is examined before designing the routing for interconnects 28/30. Tavana states "FIG. 7a illustrates an option selected by the designer and implemented by selecting a mask pattern," (Tavana, col. 6, lines 47-48) but does not indicate that the mask pattern is selected as a result of examining an specimen of the circuit with a metal one layer in the FPGA portion. Therefore, Tavana does not disclose "determining modifications to the logic design that are desired by examining an original specimen of the application specific integrated circuit with a metal one layer" and "forming a metal one layer on said semi-fabricated semiconductor wafer in the same location as the metal one layer of the original specimen but having a configuration different from the metal one layer of the original specimen to effect the desired changes."

Accordingly, Tavana does not disclose each of the aspects of claim 20, as amended, and reconsideration and withdrawal of the § 102 rejection are requested.

Dependent Claims

Claims 21-28 depend from independent claim 20, and are patentable over the art of record for at least the reasons set forth above, further in view of their additional recitations.

Conclusion

This paper does not generate any new claim fees, but a request for continued examination ("RCE") is submitted herewith. The Commissioner is hereby authorized to charge the RCE fee in the amount of $395.00 any deficiencies associated with this paper or the petition to Deposit Account No. 04-1420.

The application now stands in allowable form, and reconsideration and allowance are requested.

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